μA702A

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

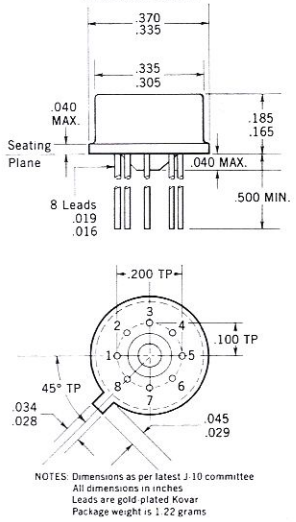
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **2500 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The μA702A is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 Volts to −6.0 V
Internal Power Dissipation	
TO-99 [Note 1]	300 mW
Flat Package [Note 2]	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

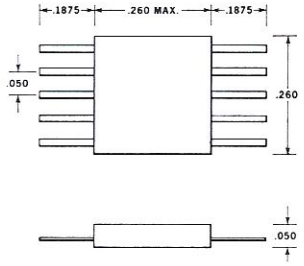
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

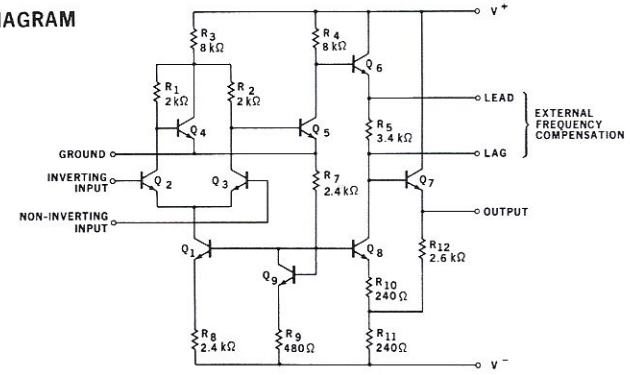
ORDER PART NO. U5B770231X†

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

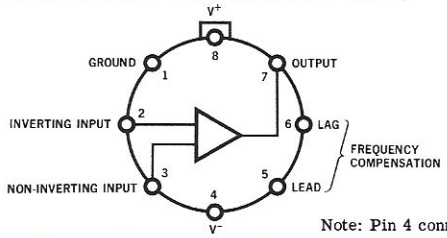


ORDER PART NO. U3H770231X

SCHEMATIC DIAGRAM

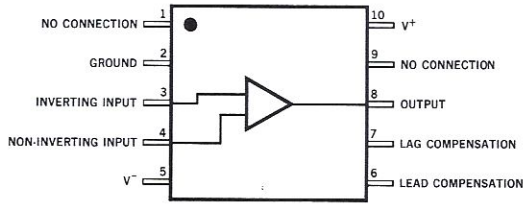


TO-99 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 4 connected to case.

FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)



Notes on page 2

* Planar is a patented Fairchild process.
† Equivalent to U5B77123IX and U3H77123IX

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

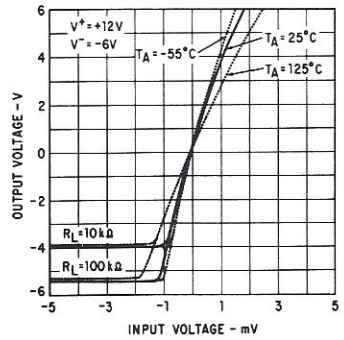
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2$ kΩ		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, f ≤ 1 kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2500	3600	6000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0.01$ μF, $R_1 = 20$ Ω, $R_L \geq 100$ kΩ, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Offset Voltage	$R_S \leq 2$ kΩ			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω, $T_A = 25$°C to $T_A = +125$°C		2.5	10		3.5	15	μV/°C
	$R_S = 50$ Ω, $T_A = 25$°C to $T_A = -55$°C		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125$°C		80	500		50	500	nA
	$T_A = -55$°C		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25$°C to $T_A = +125$°C		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25$°C to $T_A = -55$°C		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55$°C		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, f ≤ 1 kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = -6$ V to $V^+ = 6$ V, $V^- = -3$ V, $R_S \leq 2$ kΩ		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2000		7000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				500		1750	
Output Voltage Swing	$R_L \geq 100$ kΩ	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10$ kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125$°C, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55$°C, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125$°C, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55$°C, $V_{out} = 0$		90	135		19	35	mW

NOTES:

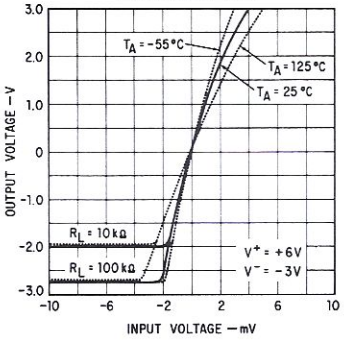
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

TYPICAL PERFORMANCE CURVES

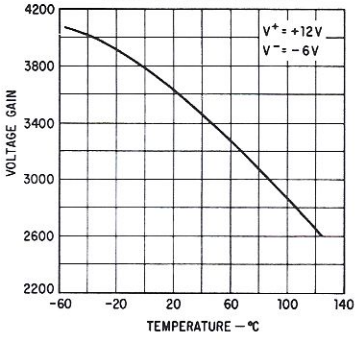
VOLTAGE TRANSFER CHARACTERISTIC



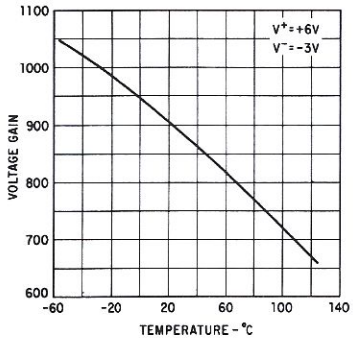
VOLTAGE TRANSFER CHARACTERISTIC



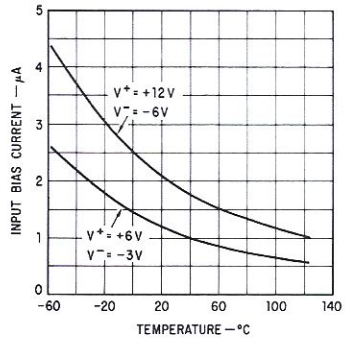
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



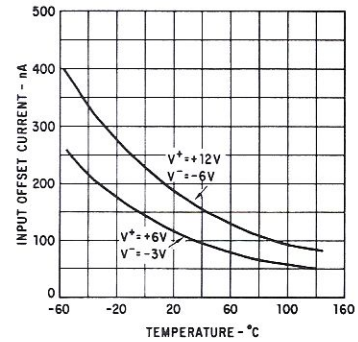
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



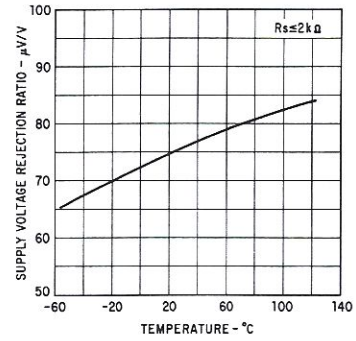
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



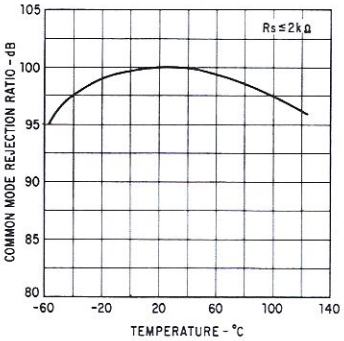
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



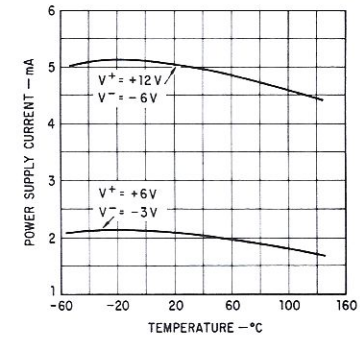
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



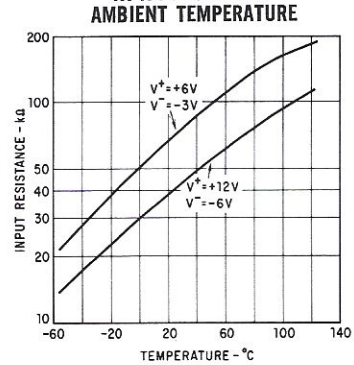
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



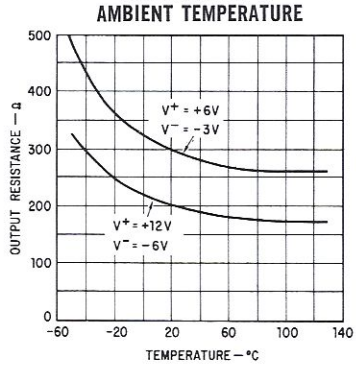
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



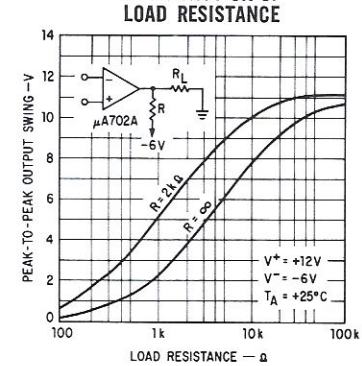
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

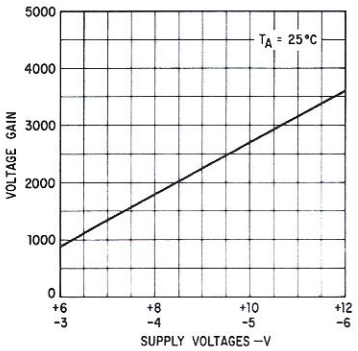


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

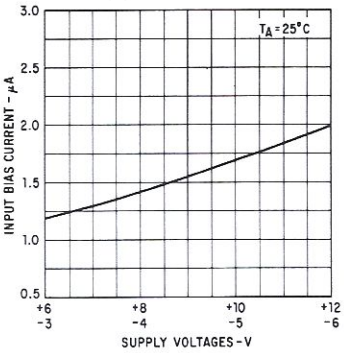


TYPICAL PERFORMANCE CURVES

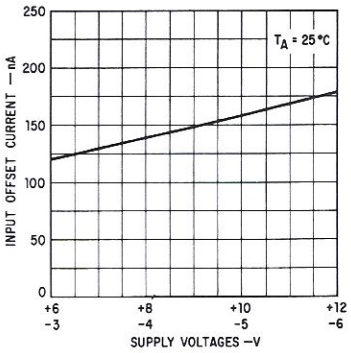
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



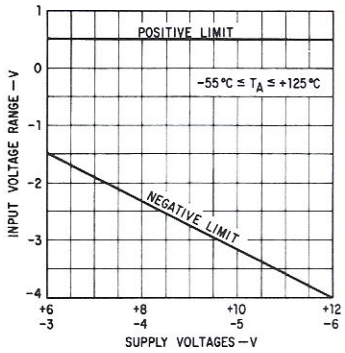
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



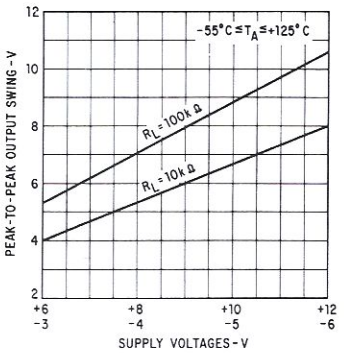
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



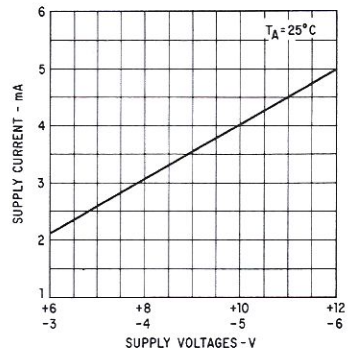
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



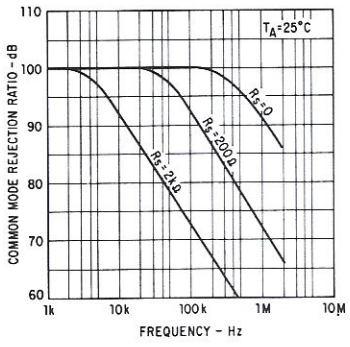
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



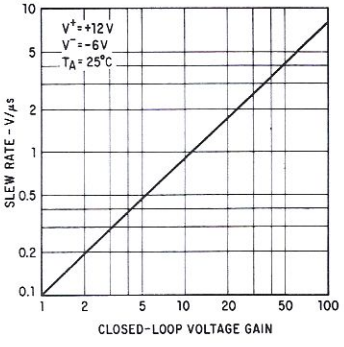
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



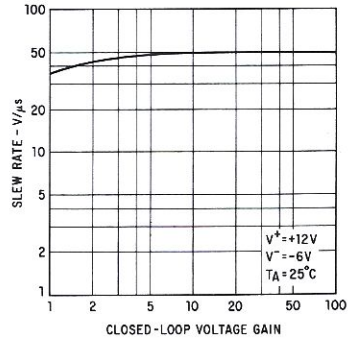
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

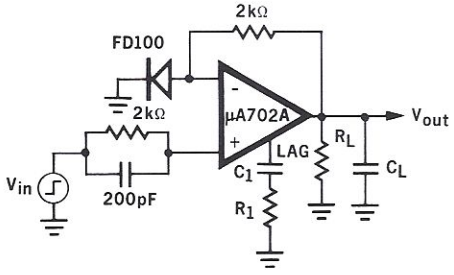


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

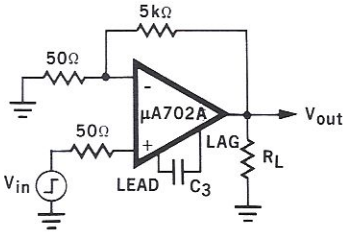


TRANSIENT RESPONSE TEST CIRCUITS

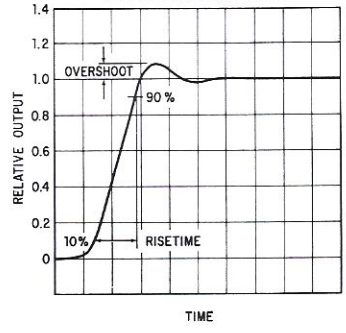
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

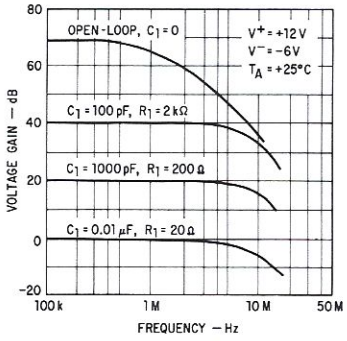
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

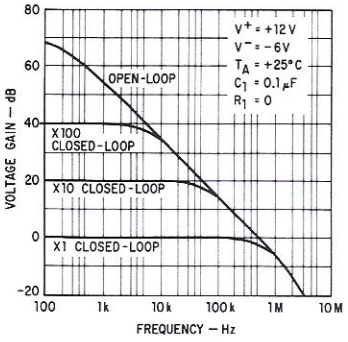
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

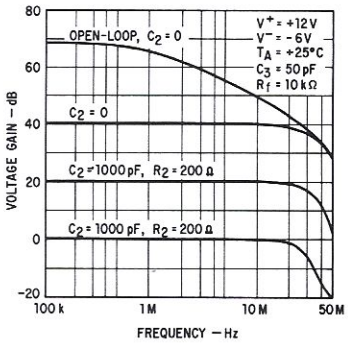
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



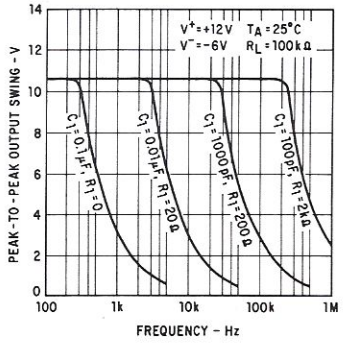
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



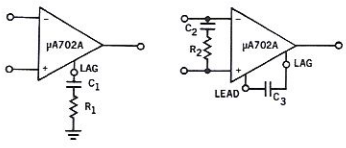
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

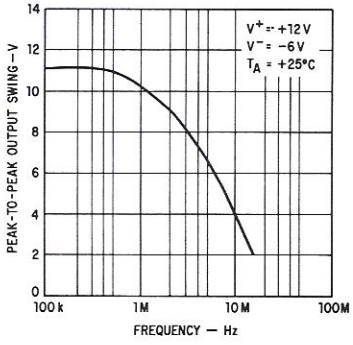


FREQUENCY COMPENSATION CIRCUITS
(Refer to Fairchild APP-117 for further details.)



LAG COMPENSATION **LEAD-LAG COMPENSATION**

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



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